WHAT IS CLAIMED IS:

1.   A storage control apparatus which is connected to a host bus connected to a CPU (Central Processing Unit), a peripheral bus connected to at least one IP (Intellectual Property), and a system memory and controls DMA (Direct Memory Access) transfer from the IP to the system memory, comprising:

.an address map judgment section which judges whether an address given from one of the peripheral bus and said host bus indicates a memory area managed by said storage control apparatus in the system memory;

a memory control section which controls data transfer to/from the system memory;

a TLB (Translation Look-aside Buffer) information holding section which holds address information that indicates an area cacheable by the CPU;

an address judgment section which judges on the basis of the address information held by said TLB information holding section whether the address given from one of the peripheral bus and the host bus indicates the area cacheable by the CPU; and

a snoop address control section which, when it is judged on the basis of a judgment result from said address judgment section that the CPU needs to be notified of the address, executes notification through the host bus.

2.   An apparatus according to claim 1, wherein when said address judgment section judges that the address indicates the cacheable area, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus.

3.   An apparatus according to claim 1, wherein said snoop address control section has a storage section

which stores addresses so as to burst-transfer the addresses to the host bus when a size of data indicated by the stored addresses has reached a burst size of the host bus.

4.   An apparatus according to claim 3, wherein when said address judgment section judges that the address indicates the cacheable area, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus.

5.   A control system capable of DMA transfer, comprising:

        a CPU connected to a host bus;

        at least one IP connected to one of the host bus and a peripheral bus;

        a system memory accessible by one of said CPU and said IP; and

        a storage control apparatus which is connected to the host bus, the peripheral bus, and said system memory and controls DMA transfer from said IP to said system memory,

        said storage control apparatus comprising

        an address map judgment section which judges whether an address given from one of the peripheral bus and the host bus indicates a memory area managed by said storage control apparatus in said system memory,

        a memory control section which controls data transfer to/from said system memory,

        a TLB information holding section which holds address information that indicates an area cacheable by said CPU,

        an address judgment section which judges on the basis of the address information held by said TLB information holding section whether the address given from one of the peripheral bus and the host bus

indicates the area cacheable by said CPU, and

a snoop address control section which, when it is judged on the basis of a judgment result from said address judgment section that said CPU needs to be notified of the address, executes notification through the host bus.

6. A system according to claim 5, wherein when said address judgment section judges that the address indicates the cacheable area, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus.

7. An system according to claim 5, wherein said snoop address control section has a storage section which stores addresses so as to burst-transfer the addresses to the host bus when the addresses corresponding to a burst size of the host bus are stored.

8. An system according to claim 7, wherein when said address judgment section judges that the address indicates the cacheable area, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus.

9. A method of controlling DMA transfer in a system comprising

a CPU connected to a host bus,

at least one IP connected to one of the host bus and a peripheral bus,

a system memory accessible by one of the CPU and the IP, and

a storage control apparatus which is connected to the host bus, the peripheral bus, and the system memory and controls DMA transfer from the IP to the system memory, comprising:

judging whether an address given from one of the peripheral bus and the host bus indicates a memory area managed by the storage control apparatus in the system memory;

when the address is in the memory area, judging on the basis of address information that indicates an area cacheable by the CPU whether the address given from one of the peripheral bus and the host bus indicates the area cacheable by the CPU; and

when it is judged on the basis of a judgment result that the CPU needs to be notified of the address, executing notification through the host bus.

10. A method according to claim 9, wherein when said address judgment section judges that the address indicates the cacheable area, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus.

11. A method according to claim 9, wherein said snoop address control section has a storage section which stores addresses so as to burst-transfer the addresses to the host bus when the addresses corresponding to a burst size of the host bus are stored.

12. A method according to claim 11, wherein when said address judgment section judges that the address indicates the cacheable area, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus.